UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,319	11/09/2001	Christopher B. Kocon	90065.141001.17732.6317.0	9637

7590 04/25/2003

Thomas R. FitzGerald, Attorney
Reynolds Arcade Bldg., Suite 210
16 E. Main Street
Rochester, NY 14614-1803

EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,319	KOCON ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- Th MAILING DATE of this communication app ars on the cov r sheet with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-23,25,27-31 and 34-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23,25,27-31 and 34-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a plurality of gate trenches, the first conductivity as N-type and the second conductivity as P-type, and the leaving of the sidewall isolation layer in place during removing of the trench mask must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is no antecedent basis in the originally filed specification for "removing said trench mask from the upper surface of said upper layer and leaving the sidewall isolation layer in place," or "forming an isolation layer of dielectric material... on said sidewall isolation layer."

3. The disclosure is objected to because of the following informalities: On page 5, line 26 "dielectric material 210" should be --gate material 210--.

Appropriate correction is required.

4. Claim 30 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The subject matter of claim 30 is encompassed by claim 29. The selected depth is defined in claim 21, from which claim 29 depends.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 21 – 23, 25, 27 – 31, and 34 – 41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With regard to claim 21, it is not clear where in the originally filed specification support for "removing said trench mask from the upper surface of said upper layer and leaving the sidewall isolation layer in place," and "forming an isolation layer of dielectric material... on said sidewall isolation layer," can be found.

With regard to claim 40, it is not clear where in the originally filed specification support for "undoped dielectric material" can be found.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 21 – 23, 25, 27 – 31, 34 – 39, and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 21 recites the limitation "the sidewall isolation layer," and "said sidewall isolation layer" in the 15th and 17th lines of the claim respectively. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action "sidewall isolation layer" will be considered --layer of dielectric material--.

10. The term "substantially coplanar" in claims 21 and 41 is a relative term which renders the claim indefinite. The term "substantially coplanar" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is not clear how coplanar the level of gate conductor is with the selected depth of the source regions. Is the level of gate conductor coplanar with the depth of the source regions? How much can the selected depth vary from being coplanar with the gate conductor?

11. With regard to claim 30, it is not clear if "a selected depth" is the same "selected depth" as defined in claim 21. Are there two selected depths?

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 21, 23, 27 – 31, and 35 – 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada (USPAT 5298780, Harada) in view of Okabe et al. (USPAT 5877527, Okabe).

With regard to claim 21, Harada discloses in figures 3 – 14 a process for forming an improved trench MOS-gated device. Harada discloses in figure 3 forming a doped upper layer (2) on a semiconductor substrate, the upper layer having an upper surface and an underlying drain region. Harada discloses in figure 4 forming a well region (3) having a first polarity in the upper layer, the well region overlying the drain region. Harada discloses in figure 5 forming a gate trench mask (23) on the upper surface of the upper layer. Harada discloses in figure 6 forming a plurality of gate trenches (40) extending from the upper surface of the upper layer through the well region to the drain region. Harada discloses in figure 7 forming sidewalls and floor in each trench comprising a layer of dielectric material (13). Harada discloses in figures 8 – 11 filling each of the gate trenches to a selected level substantially below the upper surface of the upper level with a conductive gate material (4). As far as the examiner can ascertain Harada discloses in figure 7 removing the trench mask from the upper surface of the upper layer and leaving the sidewall isolation layer in place. As far as the examiner can ascertain Harada

discloses in figure 12 forming an isolation layer of dielectric material (15a) on the upper surface of the upper layer and within the gate trench and on the sidewalls of the dielectric material, the isolation layer overlying the gate material and substantially filling the trench. Harada discloses in figure 13 removing the dielectric layer from the upper surface of the upper layer, the dielectric layer remaining within and substantially filling the trench having an upper surface that is substantially coplanar with the upper surface of the upper layer. Harada discloses in figures 12 – 13 forming a plurality of heavily doped source regions having a second polarity in the well regions, the source regions extending to a selected depth from the upper surface of the upper layer where said selected depth is substantially coplanar with the level of the conductive gate material in the trench. Harada discloses in figures 14 forming a metal contact (6) to the well and source regions over the upper surface of the upper layer. Harada does not disclose forming a plurality of heavily doped body regions having a first polarity at the upper surface of the upper layer and that the metal contacts make electrical contact to these body regions. Okabe teaches in figure 8 forming a plurality of heavily doped body regions (13a) having a first polarity at an upper surface of an upper layer (3), the body regions overlying a drain region in the upper layer. Okabe further teaches in figure 1 forming a metal contact (14) to the body and source regions (5) over the upper surface of the upper layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heavily doped body regions of Okabe in the method of Harada in order to promote electrical contact between the well regions and the overlying source-body metallization layer.

With regard to claim 23, Harada discloses in figures 3 – 14 and column 4, lines 50 – 53 wherein the upper layer comprises an epitaxial layer.

With regard to claim 24, Harada discloses in figures 3 – 14 wherein the upper layer comprises a heavily doped portion of the substrate.

With regard to claim 27, Harada discloses in figure 4 and column 4, lines 54 – 57 wherein the forming a well region comprises doping the upper layer.

With regard to claim 28, Okabe teaches in figure 8 wherein the forming heavily doped body regions comprises further doping the upper layer.

With regard to claim 29, Harada teaches in figure 12 wherein the forming heavily doped source regions comprises ion diffusing. Harada does not teach the forming heavily doped source regions comprises ion implanting. Okabe teaches in figures 7 – 10 wherein forming heavily doped source regions (5) comprises ion implanting and diffusing. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ion implanting and diffusing of Okabe in the method of Harada in order to more accurately control the doping profile and dose of the source region thereby improving device performance.

With regard to claim 30, Harada teaches in figure 12 wherein the ion diffusing is to a selected depth in the doped layer that is substantially coplanar with the filling level of the gate material in the gate trench. Okabe teaches that this is carried out by ion implanting and diffusing.

With regard to claim 31, Harada does not teach implanting the entire upper surface of the substrate with ions of the second polarity in the forming of the source regions. Okabe teaches in figures 7 – 10 implanting an entire upper surface of the substrate with ions of the second polarity (B), then forming a body mask (24) on the upper surface of the substrate, the mask comprising openings transverse to the trenches. Okabe further teaches in figures 8 and 9 wherein doping the upper surface of the substrate with a dopant of the first polarity, then removing the body mask to

form the body regions. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the blanket ion deposition of Okabe in the method of forming the source of Harada in order to more accurately control the doping profile and dose of the source region thereby improving device performance.

With regard to claim 35, Harada discloses in figure 8 and column 5, lines 10 – 12 wherein the conductive gate material within the gate trench is doped polysilicon.

With regard to claim 36, Harada discloses in figure 14 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer.

With regard to claim 37, Harada discloses in figures 4 – 14 wherein the first polarity is P and the second polarity is N.

With regard to claim 38, Harada discloses in figures 4 – 14 and column 6, lines 6 – 10 wherein the first polarization is N and the second polarization is P.

With regard to claim 39, Harada discloses in column 6, lines 6 – 10 wherein the device is a power MOSFET.

With regard to claim 40, Harada discloses in figures 3 – 14 a process for forming an improved trench MOS-gated device. Harada discloses in figure 3 forming a doped upper layer (2) on a semiconductor substrate, the upper layer having an upper surface and an underlying drain region. Harada discloses in figure 4 forming a well region (3) having a first polarity in the upper layer, the well region overlying the drain region. Harada discloses in figure 5 forming a gate trench mask (23) on the upper surface of the upper layer. Harada discloses in figure 6 forming a plurality of gate trenches (40) extending from the upper surface of the upper layer

through the well region to the drain region. As far as the examiner can ascertain Harada discloses in figure 7 forming sidewalls and floor in each trench comprising a layer of undoped dielectric material (13). Harada discloses in figures 8 – 11 filling each of the gate trenches to a selected level substantially below the upper surface of the upper level with a conductive gate material (4). Harada discloses in figure 7 removing the trench mask from the upper surface of the upper layer. As far as the examiner can ascertain Harada discloses in figure 12 forming an isolation layer of undoped dielectric material (15a) on the upper surface of the upper layer and within the gate trench, the isolation layer overlying the gate material and substantially filling the trench. Harada discloses in figure 13 removing the dielectric layer from the upper surface of the upper layer, the dielectric layer remaining within and substantially filling the trench having an upper surface that is substantially coplanar with the upper surface of the upper layer. Harada discloses in figures 12 – 13 diffusing into the surface of the substrate source dopants having a second polarity to form a plurality of heavily doped source regions that extend into the substrate along the sides of the trenches. Harada does not teach the forming heavily doped source regions comprises ion implanting. Okabe teaches in figures 7 – 10 wherein forming heavily doped source regions (5) comprises ion implanting and diffusing. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ion implanting and diffusing of Okabe in the method of Harada in order to more accurately control the doping profile and dose of the source region thereby improving device performance. Harada discloses in figures 14 forming a metal contact (6) to the well and source regions over the upper surface of the upper layer. Harada does not disclose implanting and diffusing into the surface a plurality of heavily doped body regions having a first polarity the body regions overlying the drain region in the upper layer. Okabe

teaches in figure 8 implanting and diffusing into the surface a plurality of heavily doped body regions having a first polarity the body regions overlying the drain region in the upper layer. Okabe further teaches in figure 1 forming a metal contact (14) to the body and source regions (5) over the upper surface of the upper layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heavily doped body regions of Okabe in the method of Harada in order to promote electrical contact between the well regions and the overlying source-body metallization layer.

With regard to claim 41, the combination of Harada and Okabe teach the depth of the level of the diffused implants for the source regions is substantially coplanar with the level of the conductive gate material in the trenches.

14. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada and Okabe as applied to claim 21 above, and further in view of Baba et al. (USPAT 5578508, Baba).

With regard to claim 22, it is not clear if Harada and Okabe teach wherein the substrate comprises monocrystalline silicon. Baba teaches in figure 3a and column 5, lines 4 – 8 wherein the substrate (10) comprises monocrystalline silicon. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the substrate of monocrystalline silicon of Baba in the method of Harada and Okabe in order to use a semiconductor substrate with good electrical characteristics.

15. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada and Okabe as applied to claim 21 above, and further in view of Baliga (USPAT 5323040).

With regard to claim 34, it is not clear if Harada and Okabe teach wherein the dielectric material forming the sidewalls, the floor, and the isolation layer 'in the gate trench comprises silicon dioxide. Baliga teaches in figure 2 and column 1, lines 53 – 66 wherein the dielectric material forming the sidewalls, the floor, and the isolation layer in a gate trench comprises silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the silicon dioxide of Baliga as the sidewalls, floor and isolation layer of Harada and Okabe in order to easily implement gate drive circuitry as taught by Baliga in column 1, lines 53 – 66.

16. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada and Okabe as applied to claim 21 above, and further in view of Yamamoto et al. (USPAT 5714781, Yamamoto).

With regard to claim 25, it is not clear if Harada and Okabe teach wherein the source regions surround the body regions and the source regions are separated from each other by trenches. Yamamoto teaches in figures 1a and 1b wherein source regions (4) surround body regions (17) and the source regions are separated from each other by trenches. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the source regions surrounding the body regions of Yamamoto in the method of Harada and Okabe in order to form a vertical MOSFET with a short switching time as taught by Yamamoto in column 1, lines 51 – 54.

Response to Arguments

17. Applicant's arguments filed March 11, 2003 have been fully considered but they are not persuasive.

18. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., it is not necessary to oxidize the upper portion of the polysilicon before it is removed) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

19. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
April 21, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800